CLAIMS

What is claimed is:

1. A method of driving a liquid crystal display device, the liquid crystal display device comprising driver circuit, which comprises a timing controller driven by a data transmission signal (LOAD signal)and a source driver driven by a data reception signal (DSTH signal), the method comprising the steps of:

detecting a status of the LOAD signal; and

controlling a DCLK signal according to the status of the LOAD signal.

2. A method of driving a liquid crystal display device, the liquid crystal display device comprising a driver circuit, which comprises a timing controller driven by a data transmission signal (LOAD signal)and a source driver driven by a data reception signal (DSTH signal), the method being characterized in that:

within the period from the time when the data transmission signal (LOAD signal) is enabled to the time when the data reception signal (DSTH signal) is enabled, a data clock (DCLK signal) is forced to be at a low voltage level.

3. The method of claim 2, wherein the LOAD signal is enabled at a high voltage level.

4. The method of claim 3, wherein forcing the DCLK signal to be at a low voltage level begins at the rising edge of the LOAD signal when being as a high voltage level.

5. The method of claim 3, wherein forcing the DCLK signal to be at a low voltage level begins at the falling edge of the LOAD signal when being as a high voltage level.

6. The method of claim 2, wherein the DSTH signal is enabled at a high voltage

level.

7. The method of claim 6, wherein forcing the DCLK signal to be at a low voltage level ends at the falling edge of the DSTH signal when being as a high voltage level.

8. The method of claim 6, wherein forcing the DCLK signal to be at a low voltage level ends at the rising edge of the DSTH signal when being as a high voltage level.

9. A method of driving a liquid crystal display device, the liquid crystal display device comprising driver circuit, which comprises a timing controller driven by a data transmission signal (LOAD signal)and a source driver drived by a data reception signal (DSTH signal), the method comprising the steps of:

detecting the status of the LOAD signal to determine whether the data input begins;

forcing a DCLK signal to be at a low voltage level when the LOAD signal is at a high voltage level;

detecting the status of the DSTH signal to determine whether the data input is completed; and

returning the DCLK signal to be at a normal voltage level when the DSTH signal is detected.

10. The method of claim 9, wherein the LOAD signal is enabled at a high voltage level.

11. The method of claim 10, wherein forcing the DCLK signal to be at a low voltage level begins at the rising edge of the LOAD signal when being as a high voltage level.

12. The method of claim 10, wherein forcing the DCLK signal to be at a low voltage level begins at the falling edge of the LOAD signal when being as a high

voltage level.

13. The method of claim 9, wherein the DSTH signal is enabled at a high voltage level.

14. The method of claim 13, wherein forcing the DCLK signal to be at a low voltage level ends at the falling edge of the DSTH signal when being as a high voltage level.

15. The method of claim 13, wherein forcing the DCLK signal to be at a low voltage level ends at the rising edge of the DSTH signal when being as a high voltage level.